



PTO/SB/08a/b (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	10/723,309
				Filing Date	November 26, 2003
				First Named Inventor	Christian Pacha
				Art Unit	N/A 2816
				Examiner Name	Not Yet Assigned T. LAM
				Attorney Docket Number	20046/0200609-USO
Sheet	1	of	2		

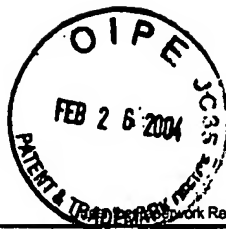
U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
u	AA	US-4,910,713-B1	03-20-1990	Madden et al.	365/189.11
u	AB	US-6,232,810-B1	05-15-2001	Oklobdzija et al.	327/217
u	AC	US-2002/0047737-A1	04-25-2002	Park et al.	327/211

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
u	BA	DE-196 15 413-A1	02-27-1997	Mashiko, Koichiro et al.		x
u	BB	DE-197 13 495-A1	10-01-1998	Berger, Horst H. et al.		x
u	BC	EP-1 170 865-A2	01-09-2002	Zama, Hidemase et al.		
u	BD	EP-1 193 871-A2	04-03-2002	Koji, Hirai		
u	BE	JP-2002-250753-A1	09-06-2002	Furuichi Masakatsu		x

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
n	CA	Hamada et al.: "Utilizing Surplus Timing for Power Reduction"; Proc. of the IEEE Custom Integrated Circuits Conference 2001; pages 89-92.	
n	CB	Inukai et al: "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration"; Proceedings of the Custom Integrated Circuits Conference, 2000; pages 409-412.	
n	CC	Shigematsu et al: "A 1-V High-Speed MTCMOS Circuit Scheme for Power-Down Application Circuits"; IEEE Journal of Solid-State Circuits, Vol. 32, No. 6, June 1997, pages 861-869.	
n	CD	P.R. van der Meer et al: "Ultra-low Standby-Currents for deep sub-micron VLSI CMOS Circuits: Smart Series Switch"; ISCAS 2000 - IEEE International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland.	
n	CE	P.R. van der Meer et al: "Effectivity of Standby-Energy Reduction Techniques for Deep Sub-Micron CMOS"; ISCAS 2001, Proceedings of the 2001 IEEE International Symposium on Circuits and Systems (ISCAS), Vol. 4, pages 594-597.	
n	CF	Huang et al: "High Performance 50 nm CMOS Devices for Microprocessor and Embedded Processor Core Applications"; Technical Digest, International Electron Devices Meeting, 2001, pages 11.1.1 -11.1.4.	
n	CG	Montanaro et al: "A 160-MHz, 32-b, 0.5-W CMOS RISC Microprocessor"; IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pages 1703-1714.	
n	CH	Hiramoto et al: "Optimum Device Parameters and Scalability of Variable Threshold Voltage Complementary MOS (VTCMOS)"; Jpn. J. Appl. Phys., Vol. 40 (2001), pages 2854-2858.	
n	CI	Zyuban et al: "Clocking Strategies and Scannable Latches for Low Power Applications"; Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)	

Examiner Signature		Date Considered	11/7/2004
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Sheet	2	of	2	Attorney Docket Number	20046/0200609-US0

	2001, August 6-7, 2001, Huntington Beach, California, USA, pages 346-351.
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